

IN THE CLAIMS

1 1. (previously amended) An integrated circuit, comprising:
2 a semiconductor substrate including semiconductor devices;
3 a first wiring layer having an associated thickness being located over the substrate and
4 having interconnect wire embedded therein;
5 a second wiring layer having an associated thickness being located on the first wiring
6 layer and having interconnect wire embedded therein; and
7 a capacitor having a first metal-based charge-storage electrode, a second metal-based
8 charge-storage electrode, and a dielectric layer interposed between the charge-storage electrodes,
9 the charge-storage electrodes extending through the thickness of the second wiring layer and at
10 least part of the first wiring layer wherein the capacitor is completely disposed in a window
11 formed through the thickness of the second wiring layer and at least part of the first wiring layer.

1 2. (original) The circuit of claim 1, wherein the dielectric layer comprises one of
2 Ta₂O₅, BaSrTiO₄, Al₂O₃, ZrO₂, and HfO₂.

1 3. (original) The circuit of claim 1, wherein
2 a first region of the substrate includes dynamic random access memory cells;
3 a second region of the substrate includes logic circuits and is physically separate from the
4 first region; and
5 the capacitor is located in a portion of the wiring layers located over the first region of the
6 substrate.

1 4. (original) The circuit of claim 3, wherein the capacitor is a functional portion of one
2 of the random access memory cells.

1 5. (original) The circuit of claim 1, further comprising:
2 a third wiring layer being located on the second wiring layer and having metal-based
3 interconnect wire embedded therein, the first charge-storage electrode of the capacitor being in
4 physical contact with a portion of the interconnect wire of the third layer.

1 6. (original) The circuit of claim 1, further comprising:
2 a tungsten plug being located between the second charge-storage electrode and a portion
3 of the substrate.

1 7. (original) The circuit of claim 1, wherein at least one of the wiring layers is a dual
2 damascene wiring layer.

1 8. (original) The circuit of claim 1, further comprising:
2 a transistor located on the substrate; and
3 a metal plug electrically connecting the second charge-storage electrode to one of a
4 source and a drain of the transistor.